IN THE CLAIMS:

The present listing of the claims replaces all prior listings:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor member having thereon a plurality of ~~interconnect pads~~ electrode terminals: and

a mounting member having a plurality of ~~electrode terminals~~ interconnect pads electrically and mechanically connected to the respective ~~interconnect pads~~ electrode terminals for mounting the semiconductor ~~chip~~ member on the mounting member,

the ~~electrode terminals~~ interconnect pads forming a plurality of I/O cells ~~each having part of the electrode terminals, the part of electrode terminals~~ including signal terminals, the I/O cells forming a first group of the I/O cells and a second group of I/O cells disposed on an inner position of the mounting member with respect to the first group.

2. (Original) The semiconductor device as defined in claim 1, wherein the semiconductor member is a semiconductor chip, the electrode terminals are internal electrodes disposed on a bottom surface of the semiconductor chip, and the mounting member is a package substrate used for packaging thereon the semiconductor chip.

3. (Currently Amended) The semiconductor device as defined in claim 1, wherein the mounting member is a semiconductor package for mounting [[a]] the semiconductor [[chip]] member on a ~~packaging~~ mounting substrate, the ~~electrode terminals are~~ semiconductor package includes ball electrodes disposed on a bottom surface of [[the]] a packaging substrate, and the

~~substrate is a~~ mounting substrate [[for forming]] forms a specified circuit by mounting the semiconductor package thereon.

4. (Currently Amended) The semiconductor device as defined in claim 1, wherein the I/O [[cell includes]] cells include only the ~~electrode~~ signals terminals ~~for signals~~ or ~~the electrode~~ terminals for signals, power and ground intermingled among one another.

5. (Currently Amended) The semiconductor device as defined in claim 4, wherein the I/O ~~cell includes~~ cells include peripherals.

6. (Currently Amended) The semiconductor device as defined in claim 1, wherein an interconnect line is electrically connected to each of the interconnect [[pad]] pads, and the interconnect lines electrically connected to the interconnect [[pad of the]] pads of at least one of the I/O cells are formed in a single interconnect layer.

7. (Currently Amended) The semiconductor device as defined in claim 6, wherein ~~the substrate includes~~ the interconnect [[pad]] pads and the interconnect [[line]] lines electrically connected to the interconnect [[pad]] pads in the single interconnect layer are formed on the surface of [[the]] a packaging substrate.

8. (Currently Amended) The semiconductor device as defined in claim 7, wherein the interconnect lines connected to the I/O cells located on inner positions extend between the I/O cells located on [[the]] an outer periphery.

9. (Original) The semiconductor device as defined in claim 6, wherein the interconnect pads and the interconnect lines electrically connected to the interconnect pads are formed as a multi-layered interconnect layer in the substrate.

10. (Original) The semiconductor device as defined in claim 9, wherein at least one of the first group and the second group includes an outer group and an inner group disposed on the inner position of the mounting member with respect to the outer group.

11. (Currently Amended) The semiconductor device as defined in claim 10, wherein the interconnect lines electrically connected to the interconnect pads corresponding to the first group of I/O cells and the interconnect lines electrically connected to the interconnect pads corresponding to the second group of I/O cells are formed in different interconnect layers.